STITCH AND SELECT IMPLEMENTATION IN TWIN MONOS ARRAY

BACKGROUND OF THE INVENTION

This application claims priority to U.S. Provisional Patent Application serial number 60/278,622, filed on March 26, 2001, which is herein incorporated by reference.

RELATED PATENT APPLICATION

now Patent No. 6,759,290

U.S. Patent Application serial number 09/810,122 filed on March 19, 2001, assigned to the same assignee as the present invention.

1) Field of Invention

The invention relates to stitching (strapping) methods of forming high-density Metal/polysilicon Oxide Nitride Oxide Silicon (MONOS) memory arrays with reduced bit line resistance, reduced control gate resistance and reduced word gate resistance using three-level metal lines, resulting in high density MONOS memory arrays with high performance.

2) Description of Prior Art and Background

Twin MONOS structures were introduced in the U.S. patent 6,255166, and U.S. Patent Applications serial numbers 09/861,489 and 09/595,059 by Seiki Ogura et al. and also various array fabrication methods of the twin MONOS memory array were introduced in U.S. Patents 6,177,318 and 6,248,633 B1 and U.S. Patent Application serial number 09/994,084 filed on November 21, 2001.